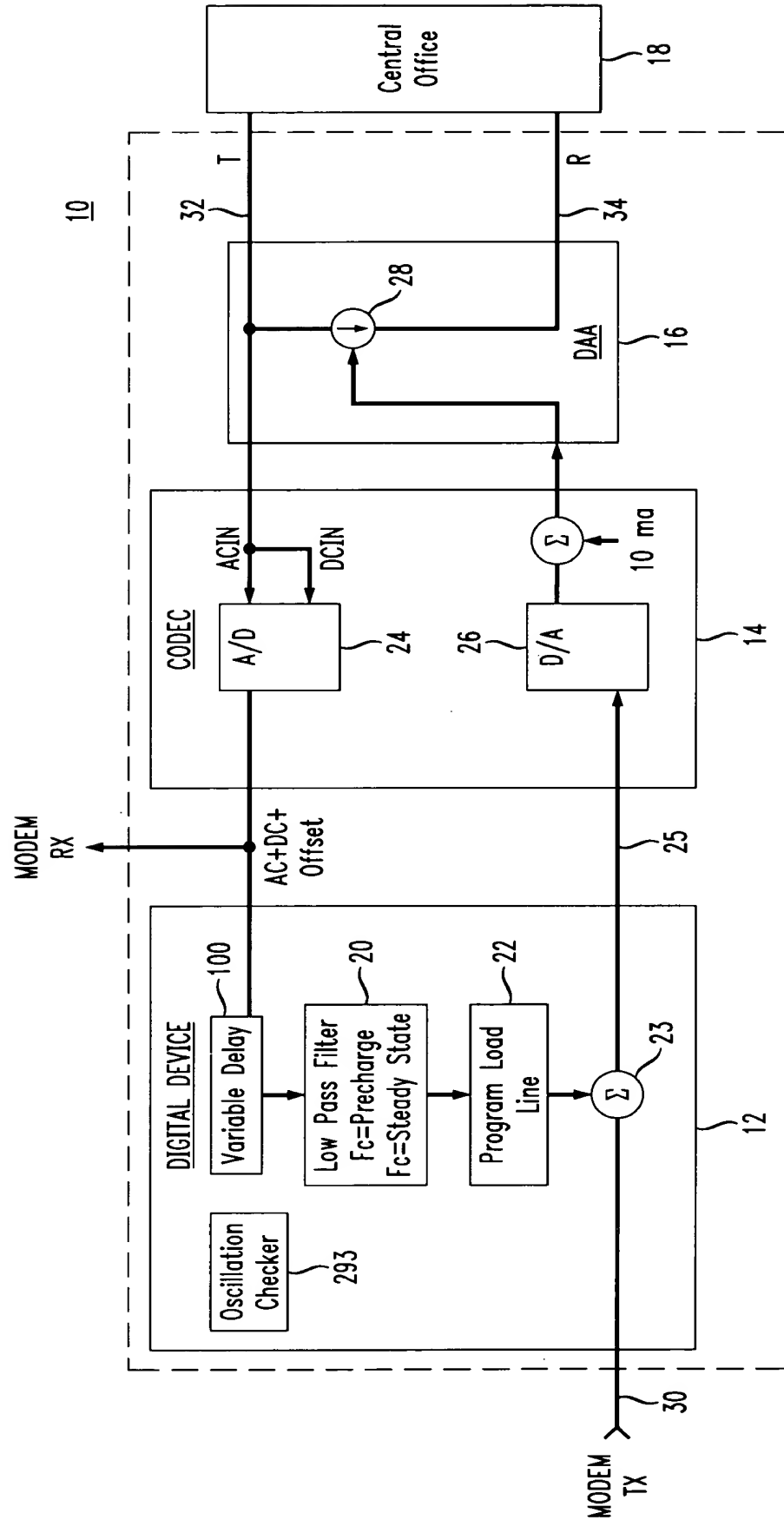


FOUO 0404060

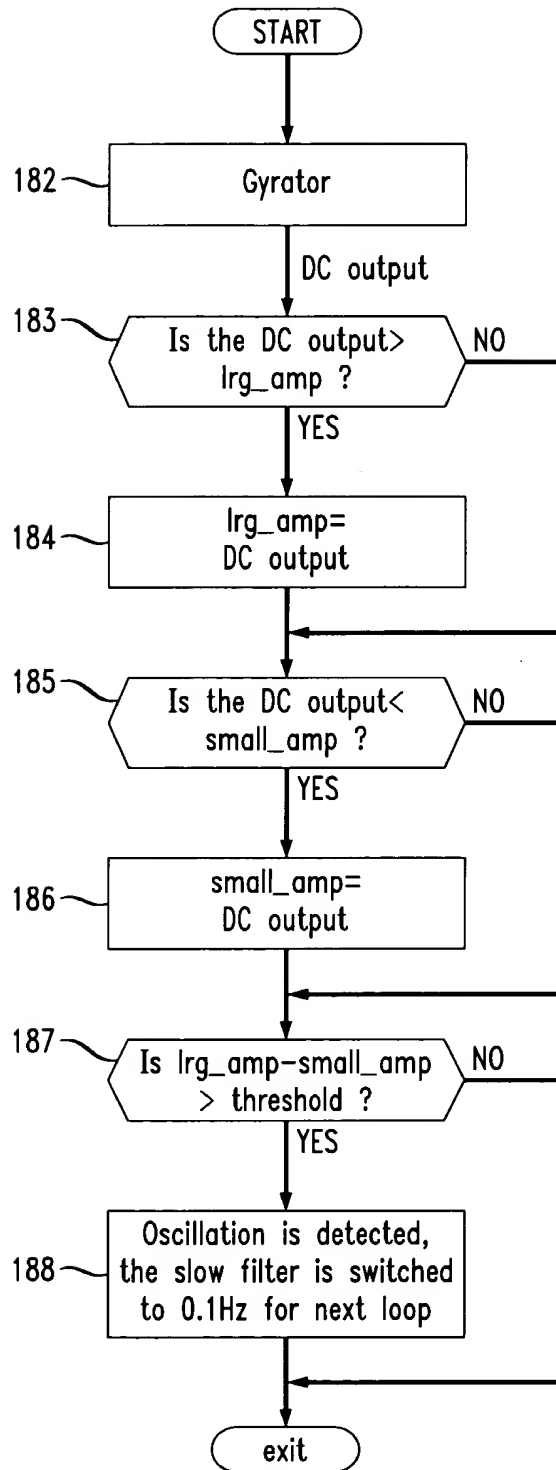
FIG. 1A

DYNAMICALLY ADJUSTABLE DIGITAL GYRATOR HAVING EXTENDED FEEDBACK



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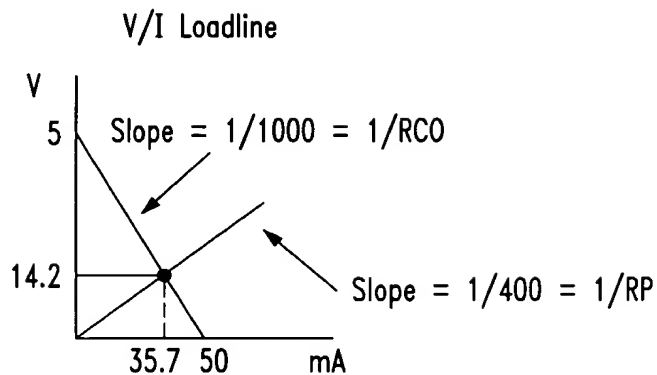
FIG. 1B



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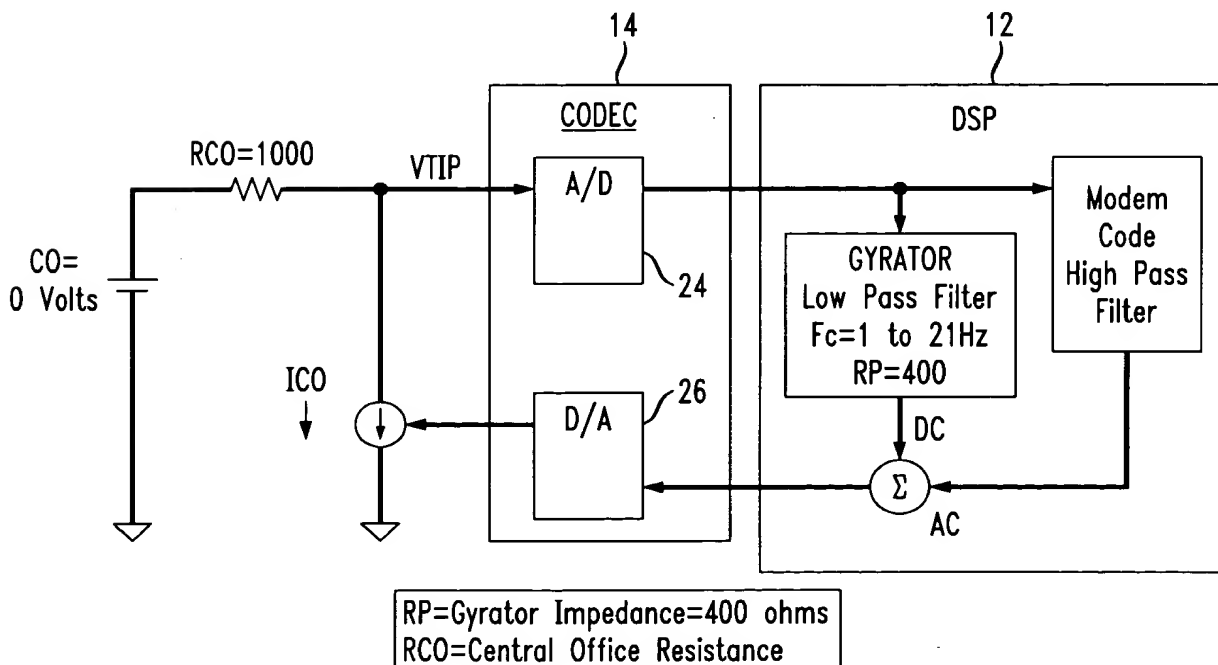
FIG. 2A



$50 - I_{CO} \cdot R_{CO} = I_{CO} \cdot R_P = V_P$
 $I_{CO} = 14.27 \text{ mA}$
 $V_P = 35.7 \text{ Volts}$
 Note: All results are at steady state

FIG. 2B

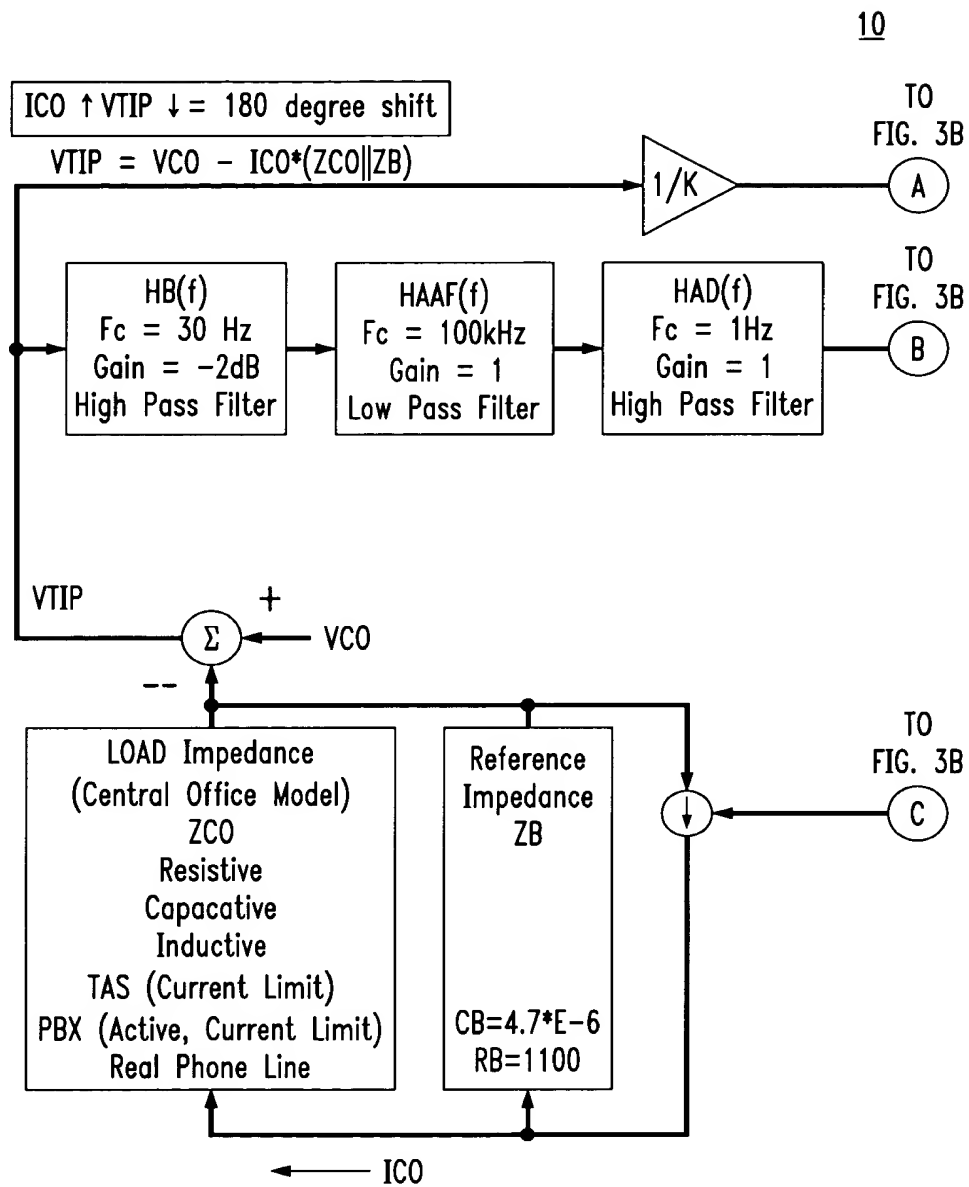
DYNAMICALLY ADJUSTABLE DIGITAL GYRATOR EXAMPLE



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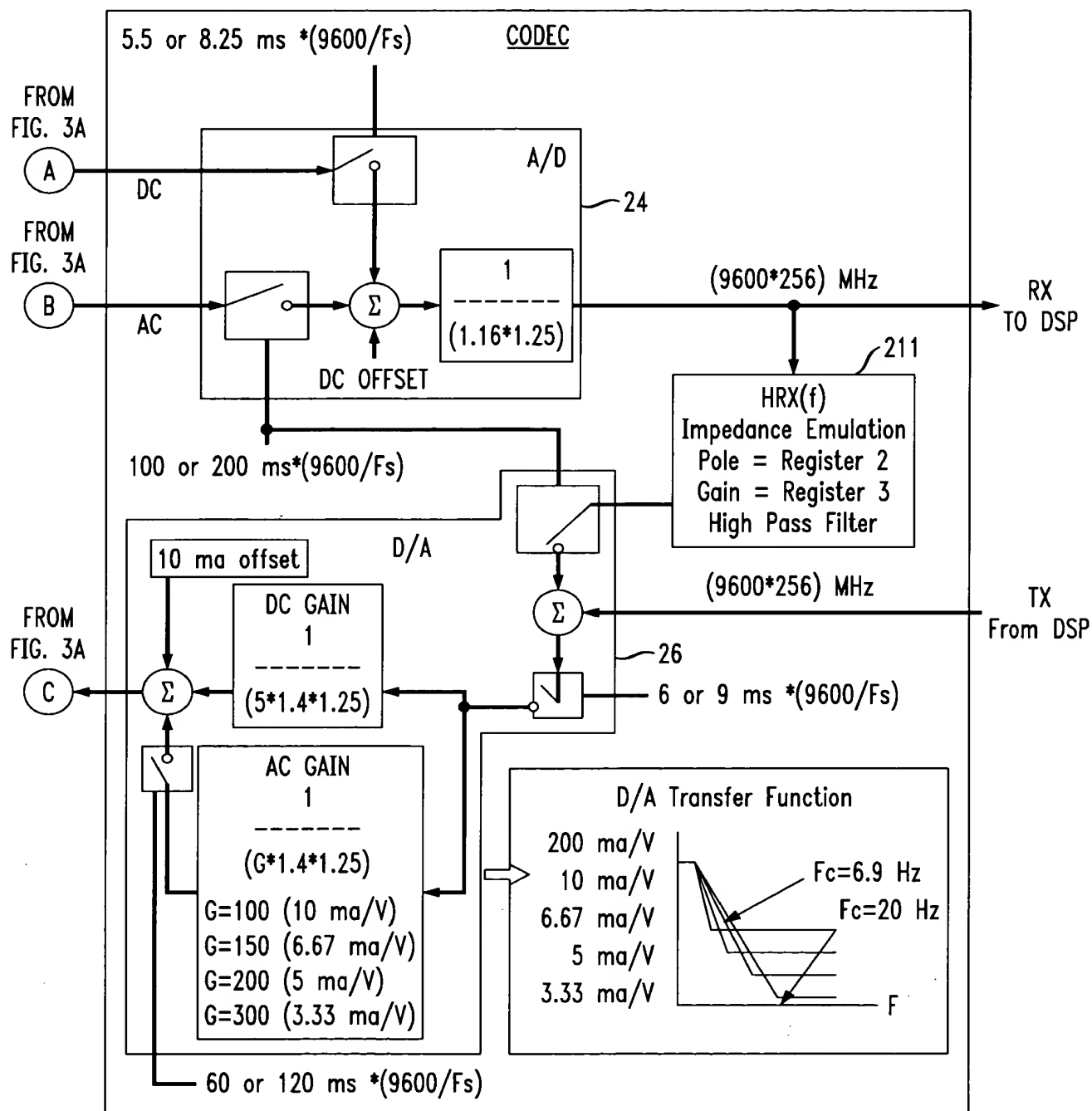
FIG. 3A

CODEC and Telephone System Stability Block Diagram



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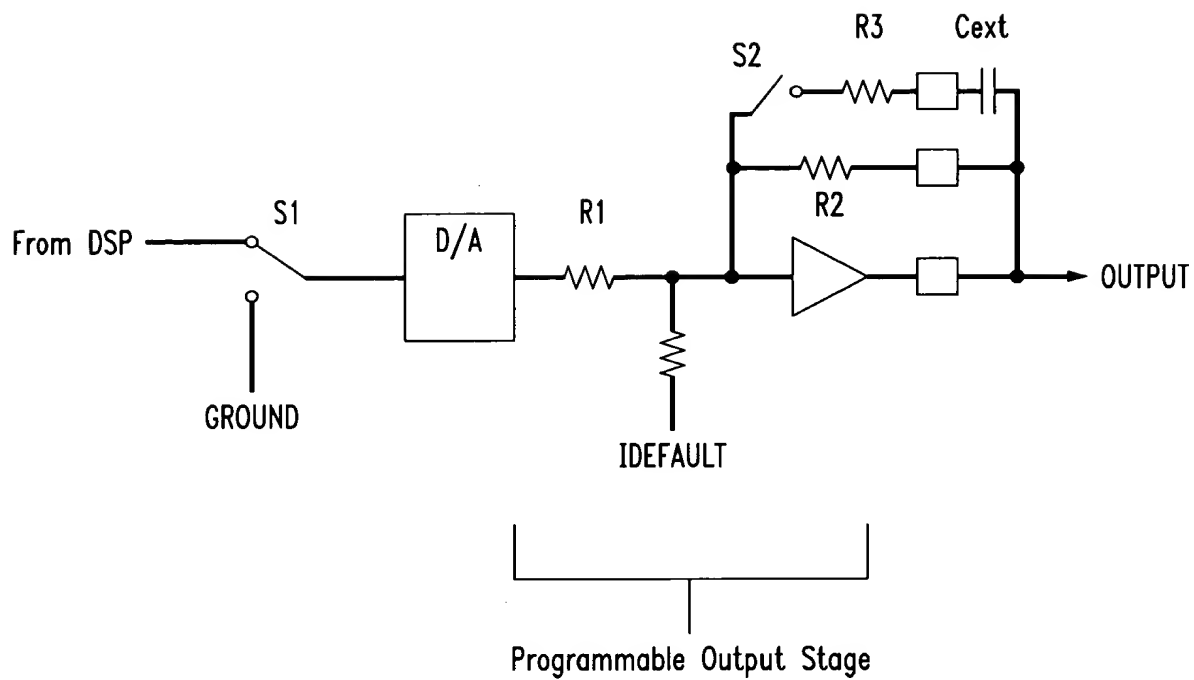
FIG. 3B



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FIG. 4

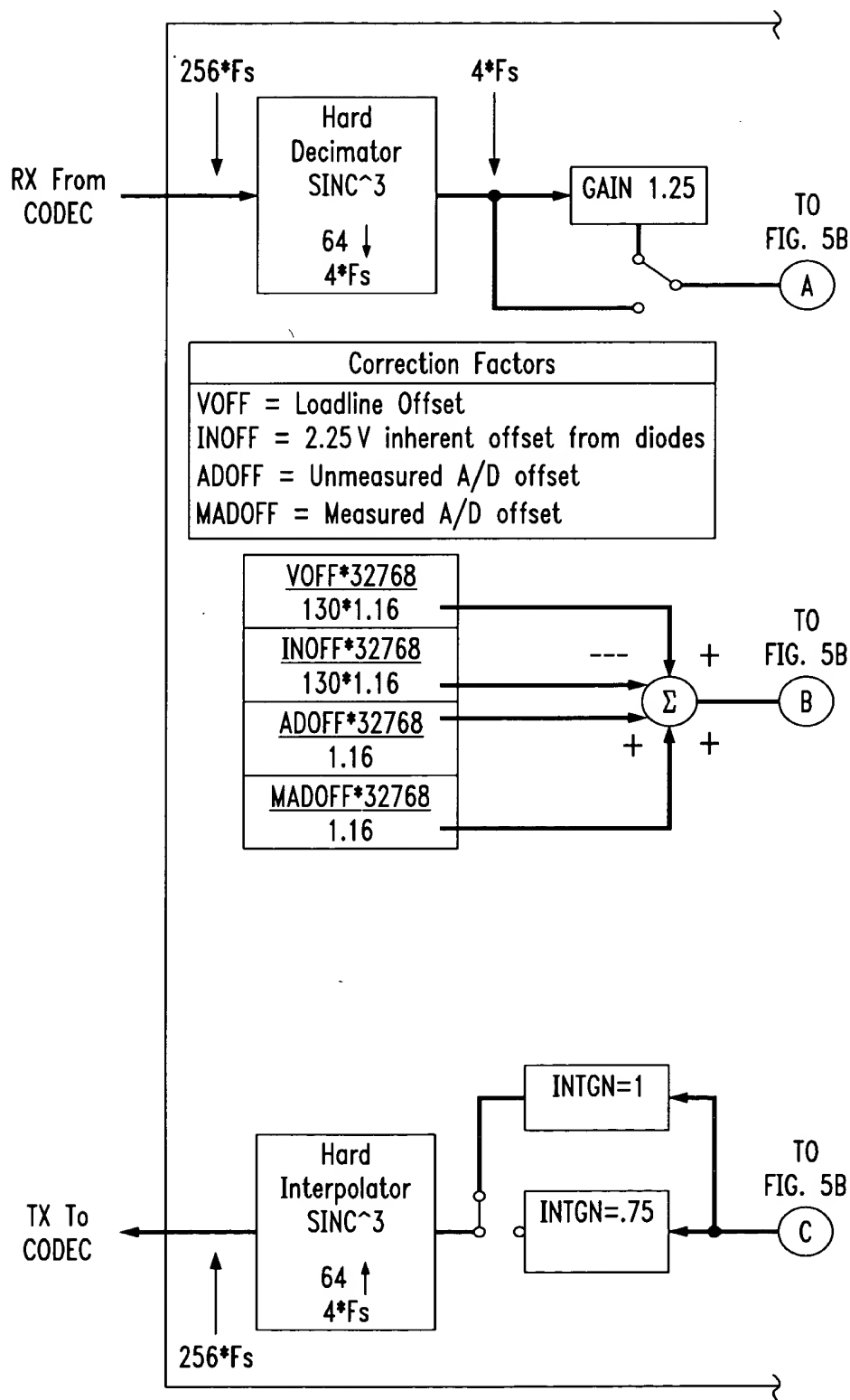
Simplified D/A Path



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FIG. 5A

DSP Based Gyrator Block Diagram



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FIG. 5B

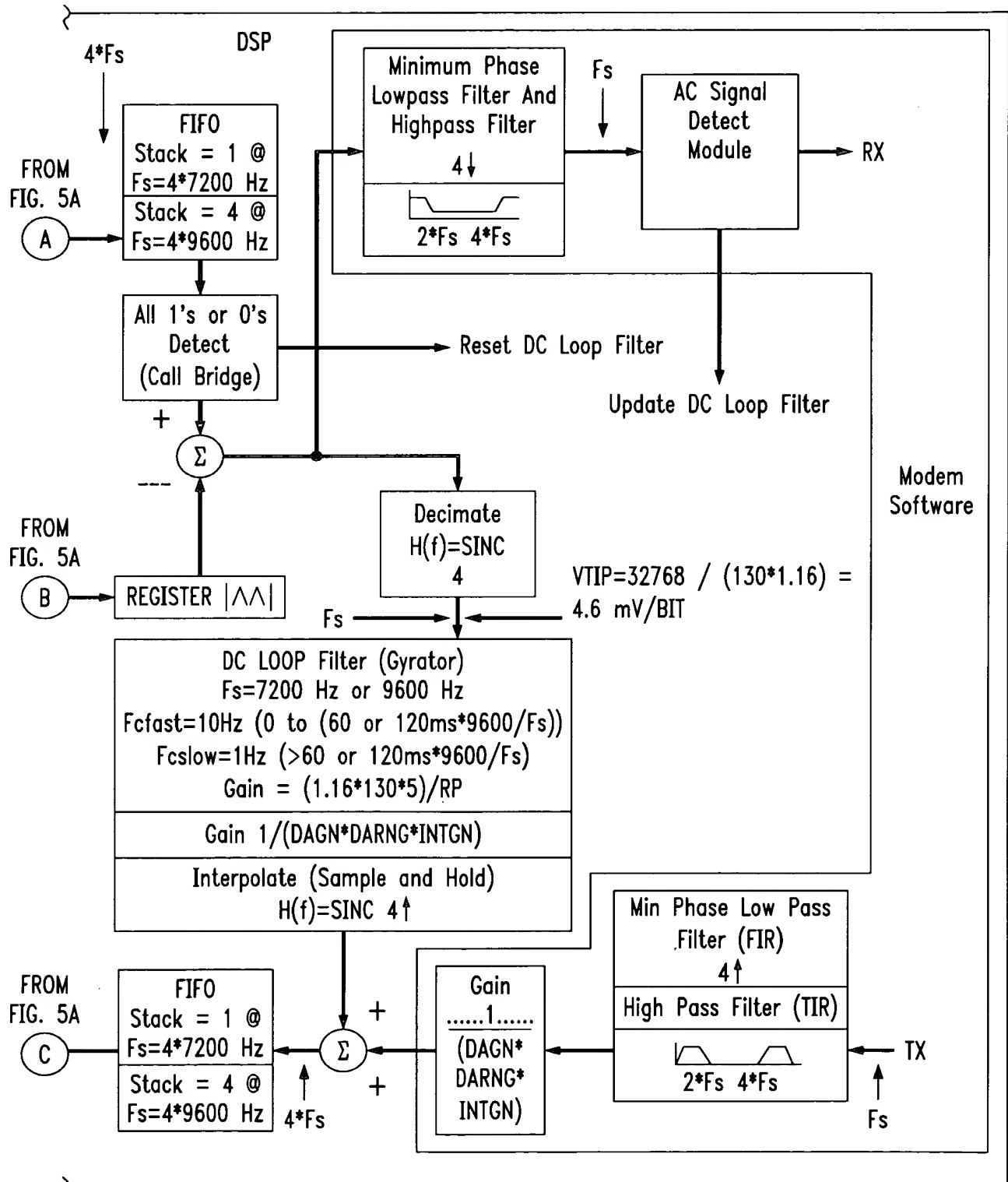


FIG. 6

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ADRNG= 1.16
DCDIV= 130
DCGN= 5
DAGN= 1.25
DARNG= 1.4
INTGN= .75

Input @ 4.6V/LSB @TIP

1 / (.005*32768)=.00611 mA/LSB

Input Gain
 $\frac{ADRNG * DCDIV * DCGN * Filtgain}{Resistance}$

FAST GAIN
Register High Word
Register Low Word

SLOW GAIN
Register High Word
Register Low Word

$$H(z) = \frac{\text{Input Gain}}{1 - \text{POLE} * Z^{-1}}$$

Feedback Gain
FAST POLE
Register High Word
Register Low Word

SLOW POLE
Register High Word
Register Low Word

Σ
+
Positive Current Limit
Register
Current Limit*.00611 ma/LSB
If I > Current Limit set I=Current Limit
Hysteresis
Z⁻¹
Precharge Current
Register High Word
Register Low Word

CODEC Default Current
i i ma /.00611 ma/BIT = 0x708
Register

Σ
--
Negative Clipper
If<0 Output = 0

Output Gain
1 / (DAGN * DARNG*INTGN)

Sample and Hold
4X
Register

Data Out

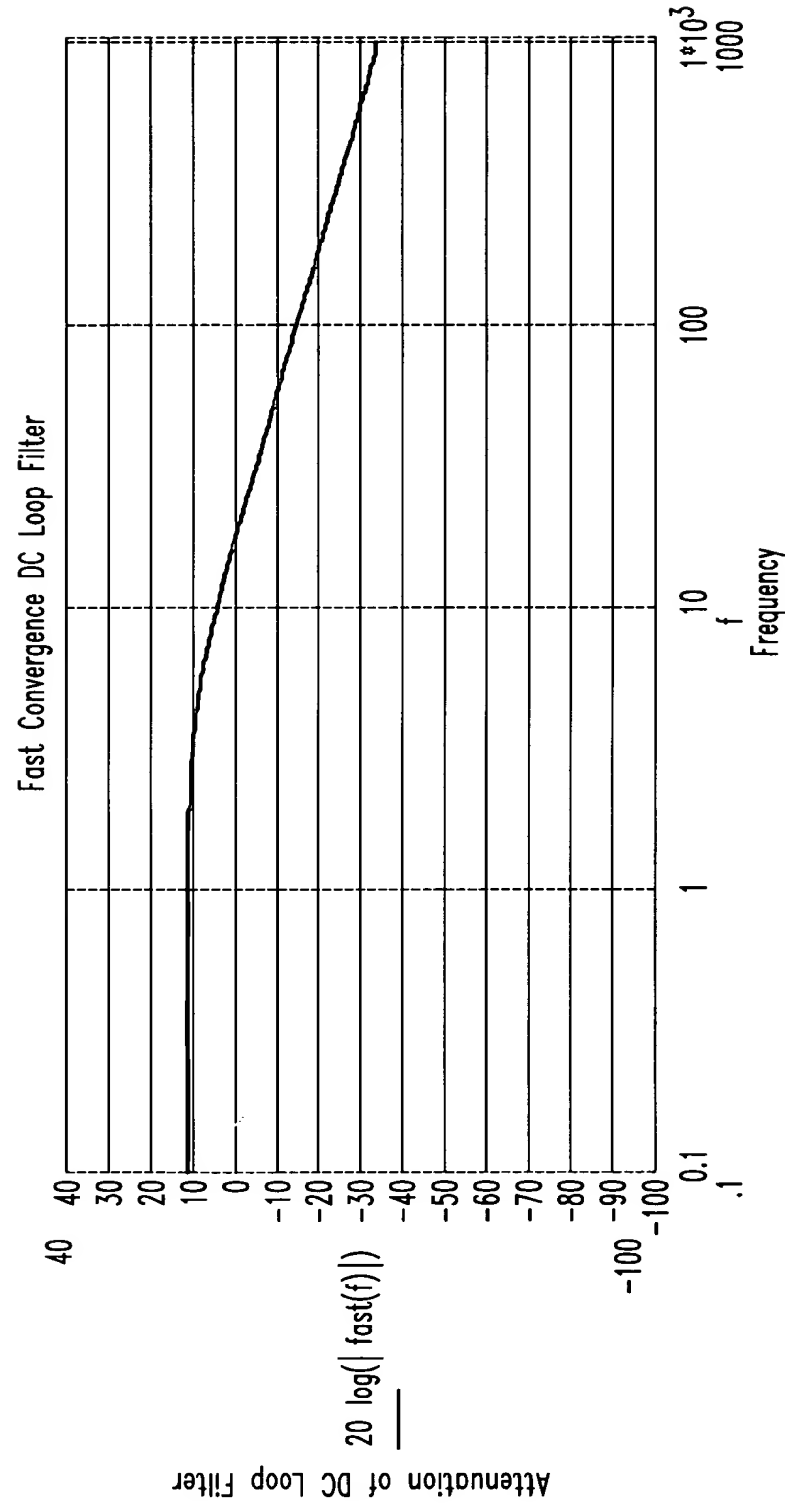
For 2000-04-09

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APPROVED C.G. FIG.
CLASS SUBCLA

FIG. 7A



TOT 260 04042860

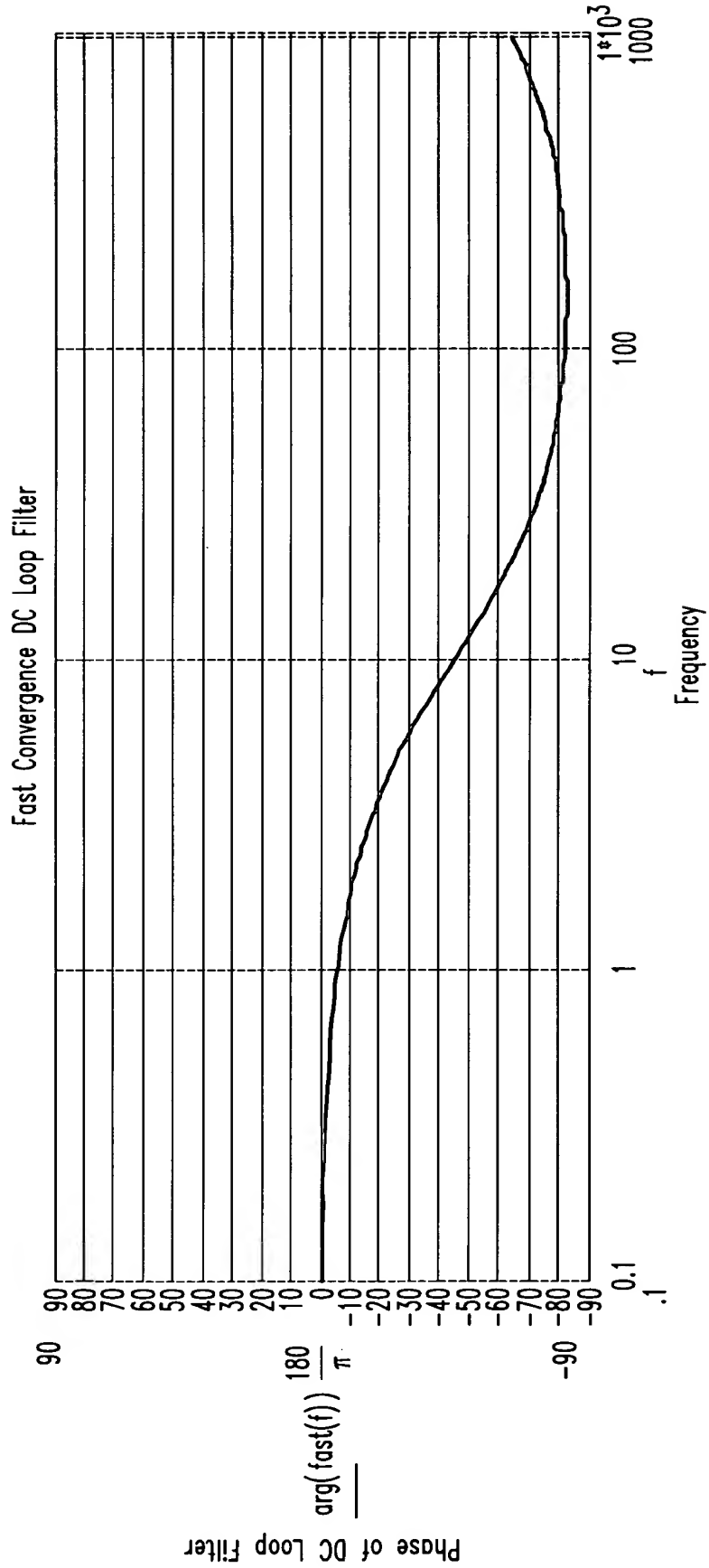
APPROVED: G. FIG.
CLASS: SUBCLASS:
DATE:

CUI 1-27

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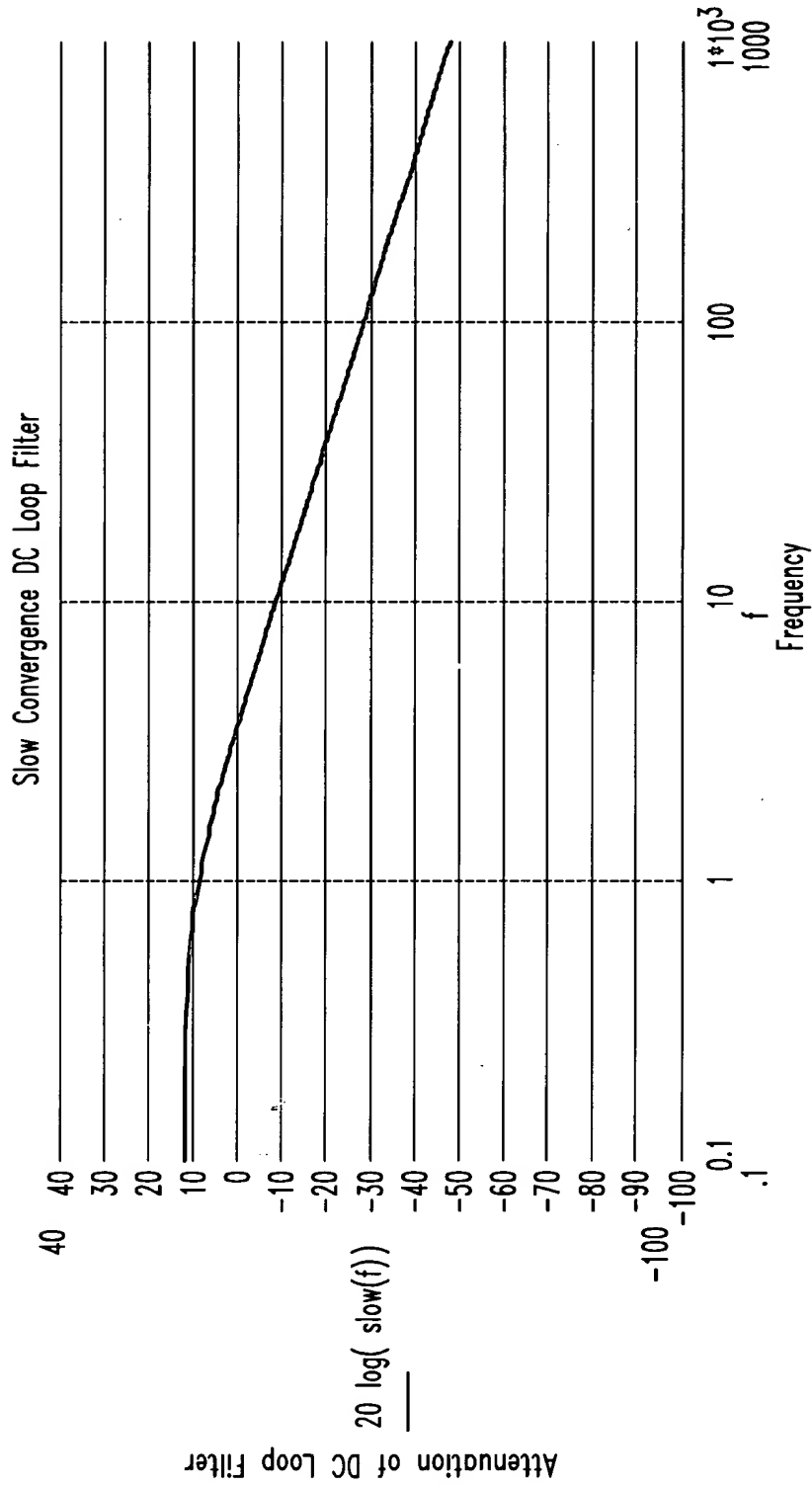
FIG. 7B

10 Hz Fast DC Loop Filter Gain and Phase



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FIG. 8A



FORM 260-01010000

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CLASS SUBCLASS
O.G. FIG.

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FIG. 8B

1 Hz Slow DC Loop Filter Gain and Phase

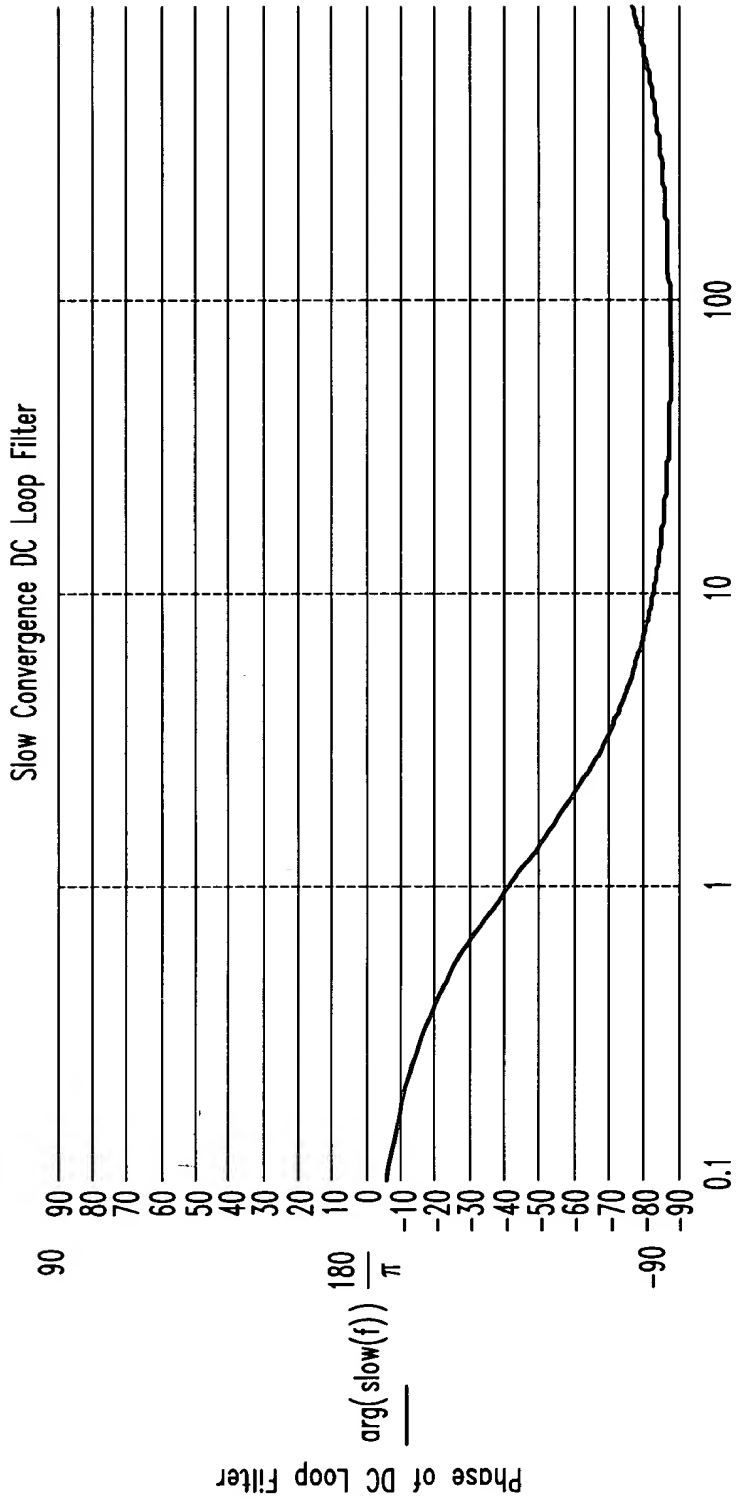


FIG. 9

First Order Filter Topology

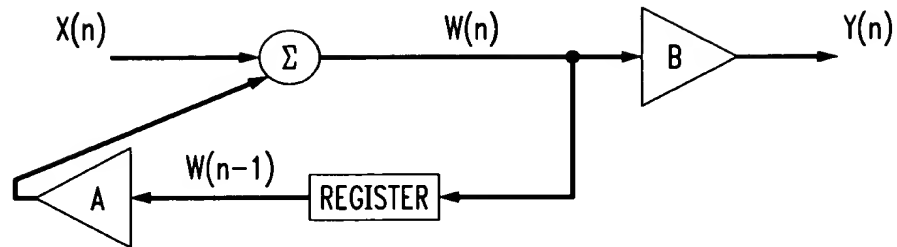
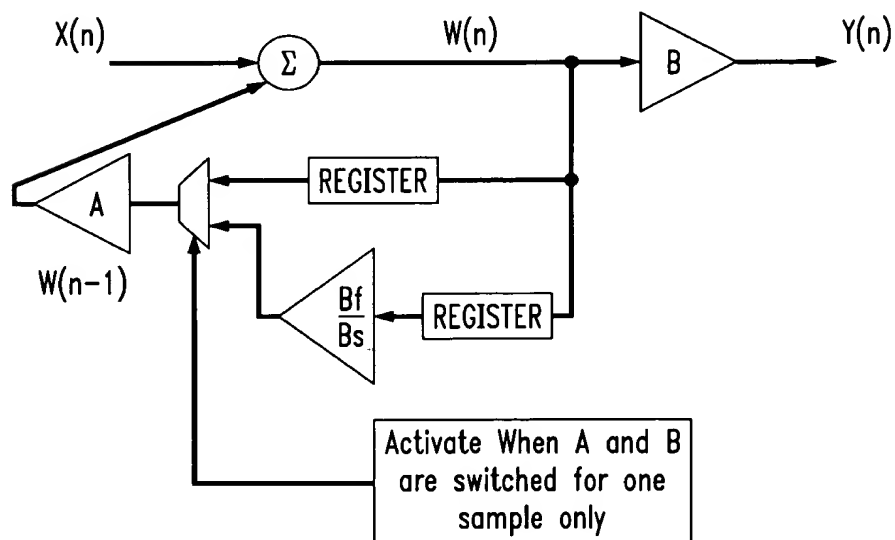


FIG. 10

Final Low Pass Topology with glitch removed

[illegible]

101250 " 0101880

APPROVED	C.G. FIG.
BY	CLASS/SUBCLASS
DR. FISMAN	

CUI 1-27

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FIG. 11A

DC Loop Filter Without Hysteresis

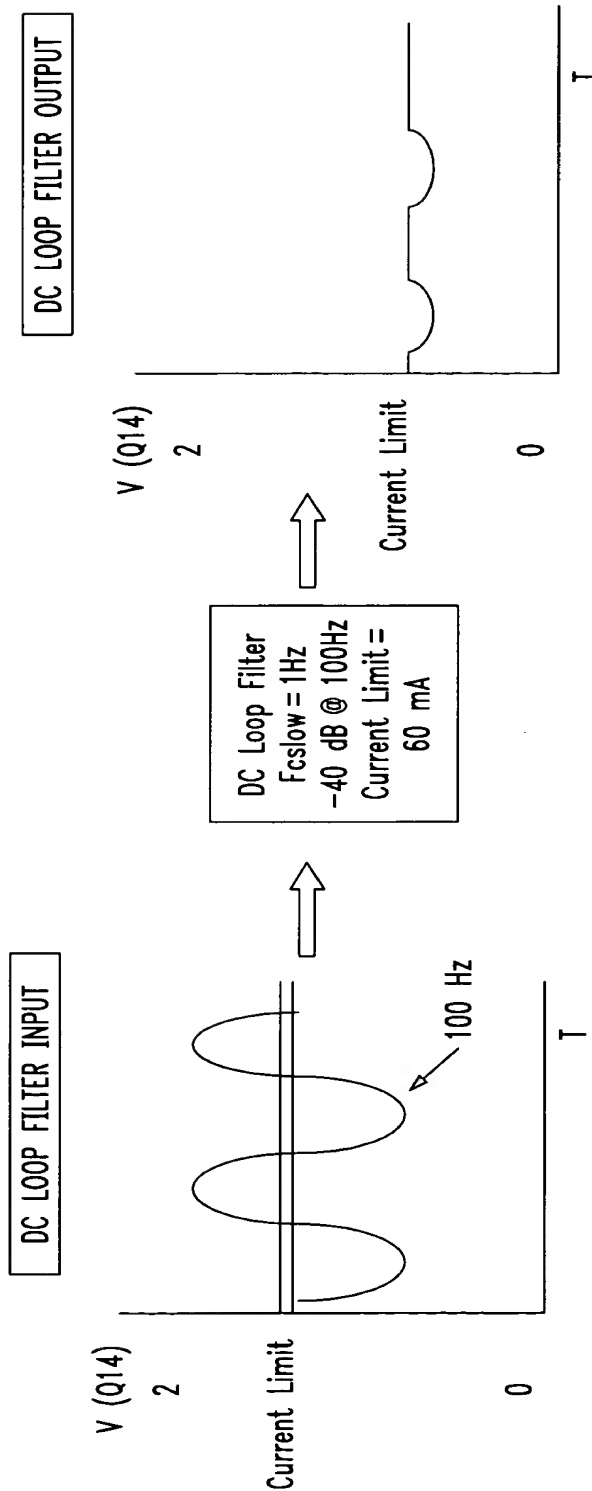


FIG. 11B

DC Loop Filter With Hysteresis

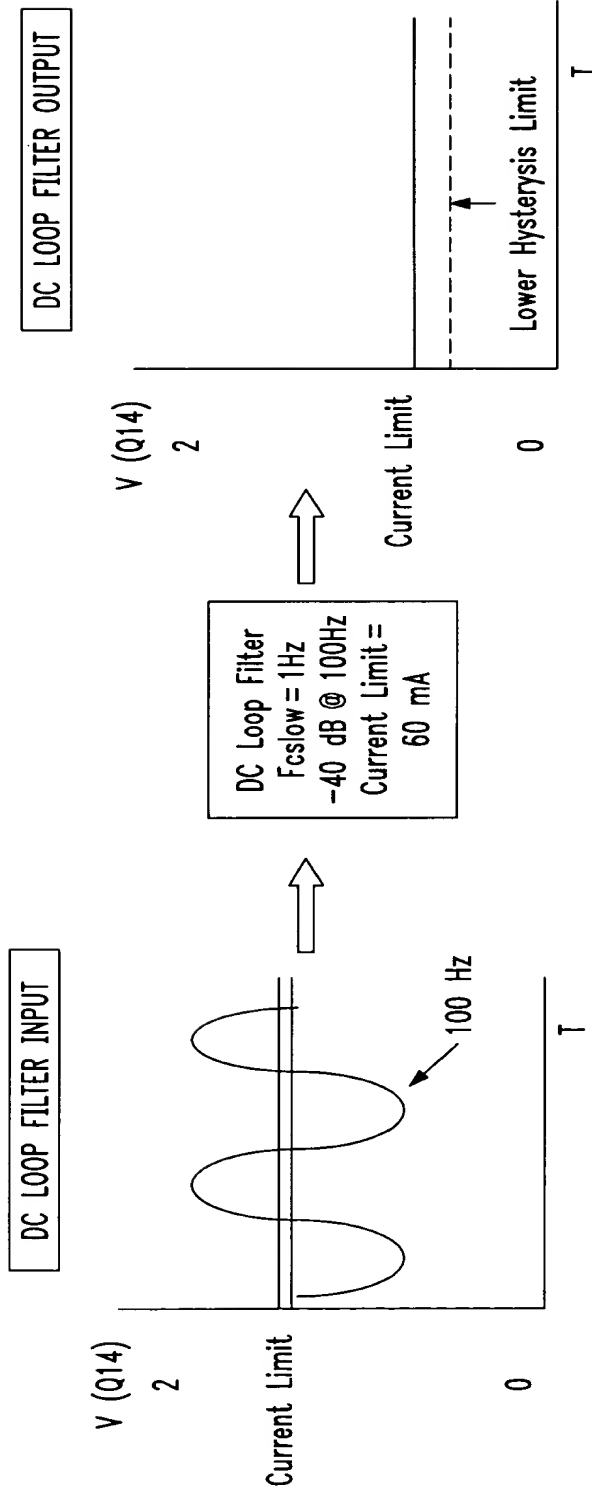


FIG. 12B

TAS, PBX and Real Phone Line V/I Loadlines

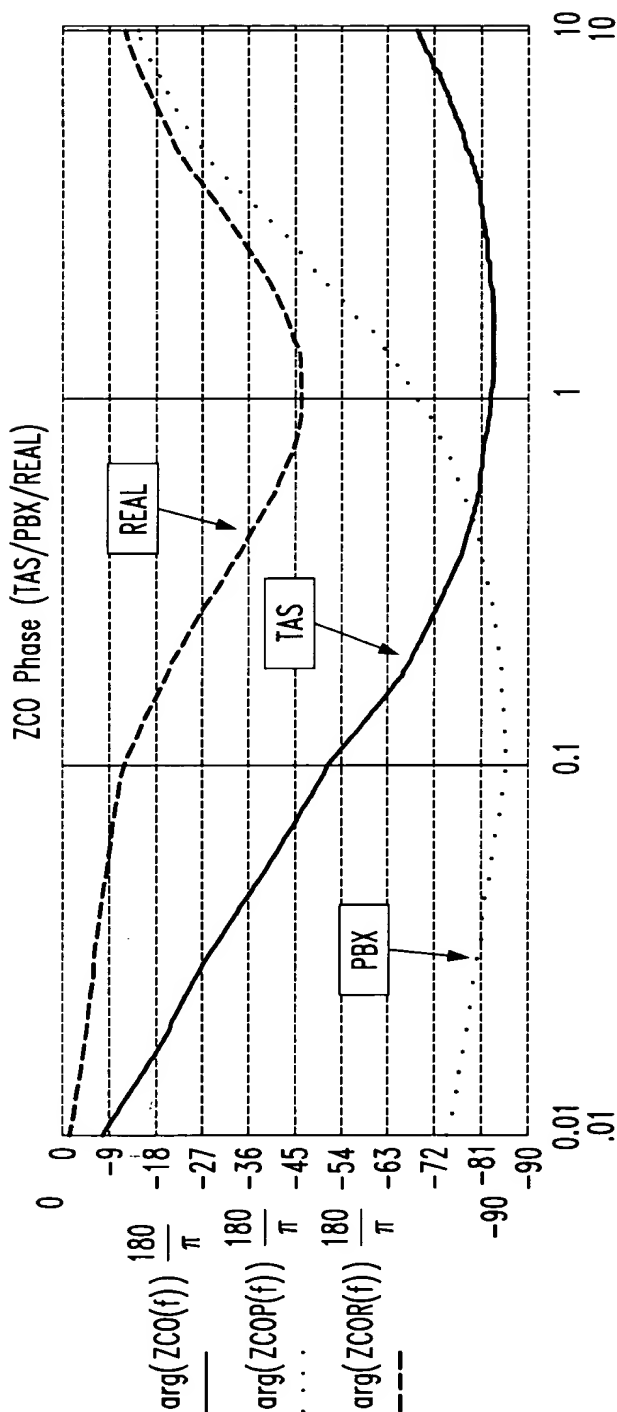


FIG. 13A

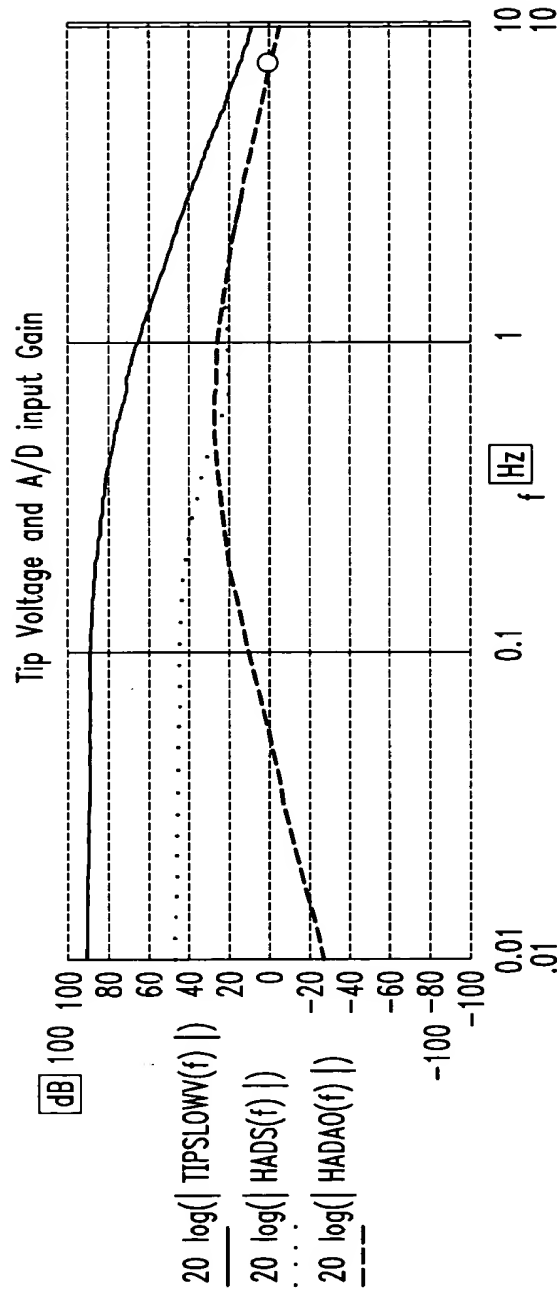
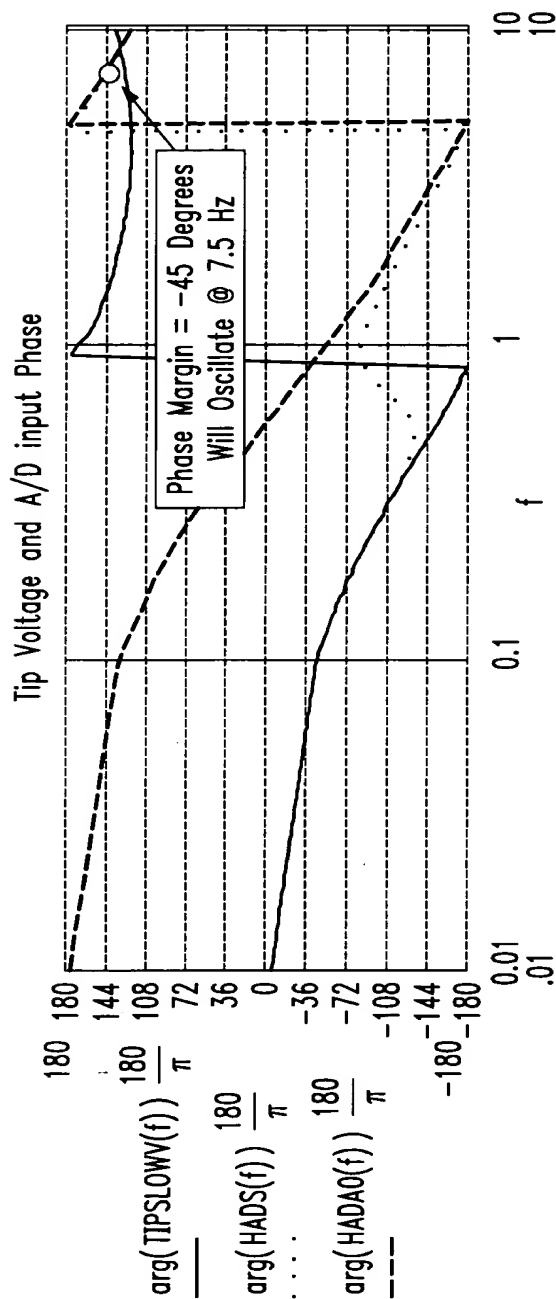


FIG. 13B

TAS Termination with Lowpass Filter Cutoff = 1 Hz



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FIG.
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FIG. 14A

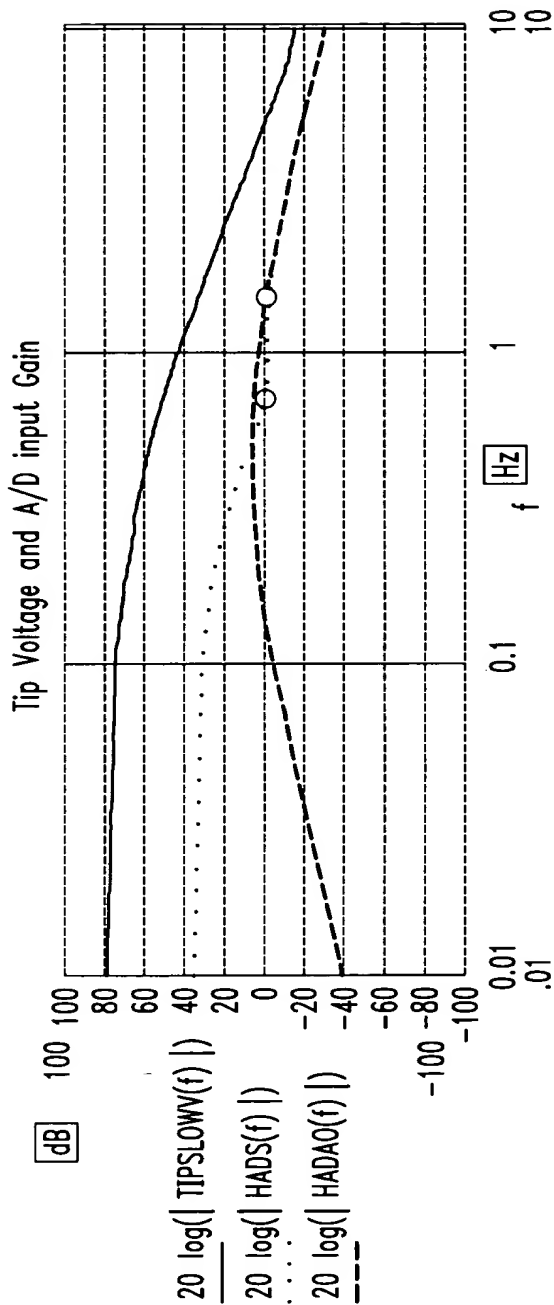
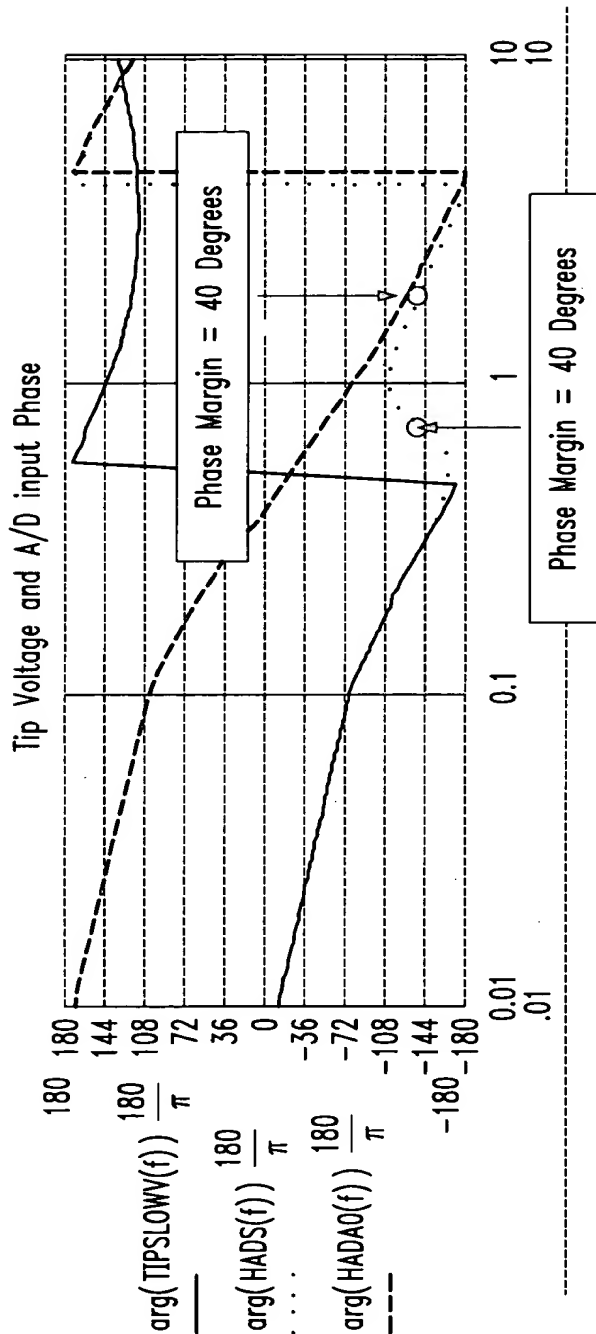
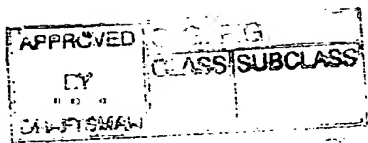


FIG. 14B

TAS Termination with Lowpass Filter Cutoff = .1 Hz





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FIG. 15

PRIOR ART

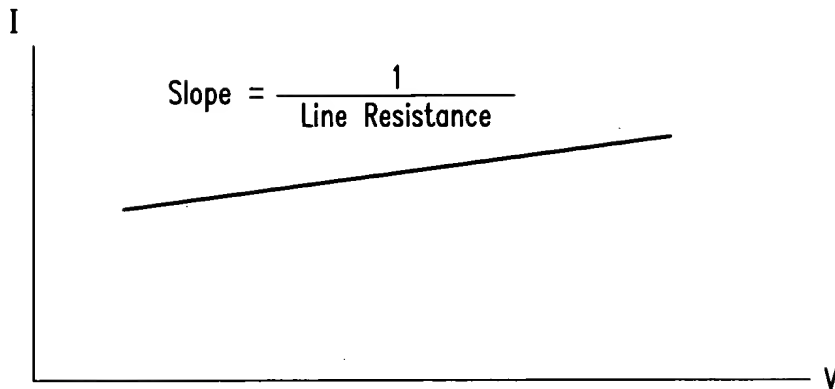


FIG. 16

PRIOR ART

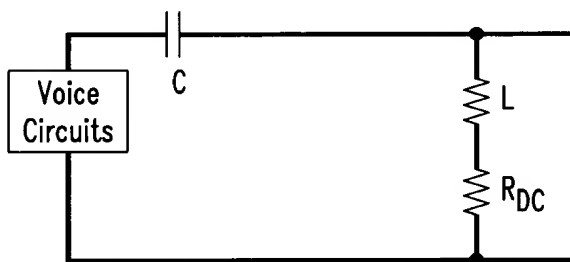
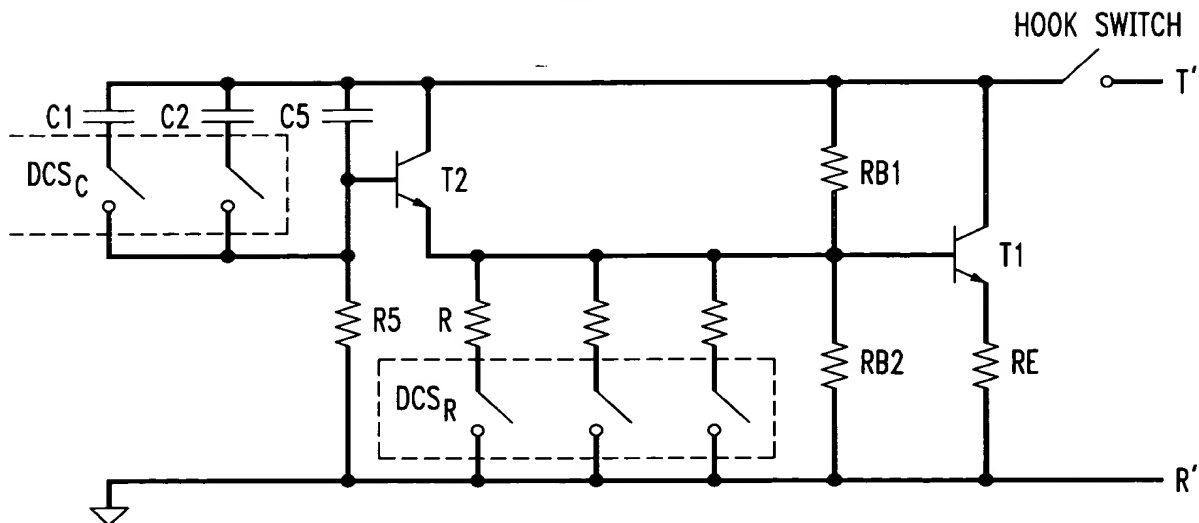


FIG. 17

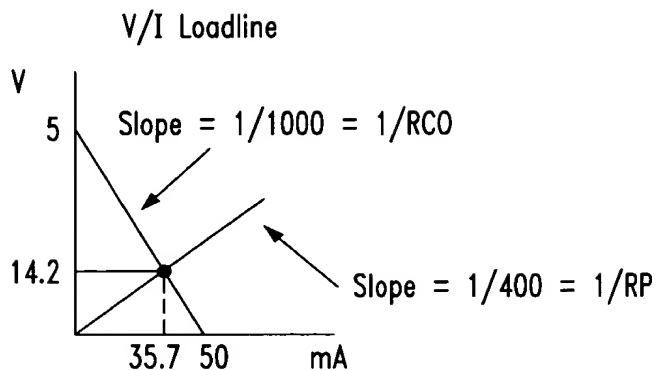
PRIOR ART



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FIG. 18A

PRIOR ART



$$50 - ICO * RCO = ICO * RP = VTIP$$

$$ICO = 14.27 \text{ mA}$$

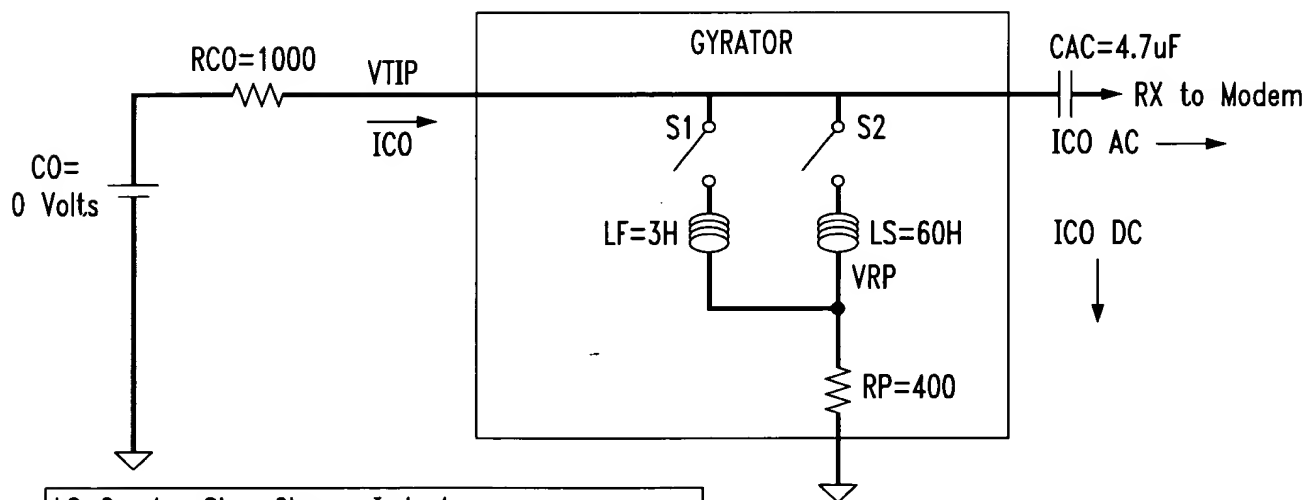
$$VP = 35.7 \text{ Volts}$$

Note: All results are at steady state

FIG. 18B

PRIOR ART

Basic External Gyrator Example



LS=Gyrator Slow Charge Inductor
LF=Gyrator Fast Charge Inductor
RP=Gyrator Impedance
CAC=AC coupling capacitor for AC modem signals
RCO=Central Office Resistance

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